PATENT APPLICATION
Docket No. 9898-217

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Jae-Hyun Joo and Wan-Don Kim		
Serial No.	10/055,270	Examiner:	Mai, Anh D
Confirmation No.	6757		
Filed:	January 22, 2002	Art Unit:	2814
For:	METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE HAVING A METAL-INSULATOR-METAL CAPACITOR		

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S AMENDED BRIEF
UNDER 37 CFR §1.192

Appeal is taken from the Examiner's Office Action mailed September 8, 2003, finally rejecting claims 1, 2, 4, 6-15, 17-20 and 24-32, in the instant application.

This Appeal Brief is in furtherance of the Notice of Appeal mailed in this case on November 7, 2003, and is responsive to Examiner's Notice of Defective Appeal.

The fees required under §1.17(c) and any required petition for extension of time for filing this Brief and fees therefore are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This Brief is transmitted in triplicate.

This Brief contains these items under the following headings, and in the order set forth below.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST
37 CFR §1.192(c) (1)

The real party in interest is the assignee of the present application – Samsung Electronics, Ltd. of Kyungki-do KOREA.

II. RELATED APPEALS AND INTERFERENCES
37 CFR §1.192(c) (2)

The Board's decision in the present Appeal will not directly affect, or be directly affected, or have any bearing on any other appeals or interferences known to the appellant, or to the appellant's legal representative.

III. STATUS OF CLAIMS
37 CFR §1.192(c) (3)

Claims 7, 8, 24 and 25 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor(s), at the time the application was filed, has possession of the claims invention.

Claims 7, 18 and 24-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention.

Claims 1, 2, 4, 6-15, 17-20, 24, 25 and 30-32 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Agarwal et al., (U.S. Publication No. 2002/0037630) of record in view of Applicant admitted prior art.

- Claims presented for Appeal: 1, 2, 4, 6-15, 17-20, 24, 25 and 30-32
- Claims withdrawn from consideration but not cancelled: NONE
- Claims canceled: 26-29
- Claims pending: 1, 2, 4, 6-15, 17-20 and 24-32

  of which:

  a. claims allowed: NONE

  b. claims rejected: 1, 2, 4, 6-15, 17-20 and 24-32

Rejected claims, namely claims 1, 2, 4, 6-15, 17-20, 24, 25 and 30-32, are being appealed. The appealed claims are eligible for appeal, having been finally rejected.

IV. STATUS OF AMENDMENTS
37 CFR §1.192(c) (4)

Subsequent to the last Office Action mailed on Sept. 8, 2003, which contained a Final Rejection of the appealed claims, no amendment has been filed.

V. SUMMARY OF THE INVENTION
37 CFR §1.192(c) (5)

The claimed invention is directed to a method for forming a capacitor structure on a semiconductor device where the lower electrode of the capacitor structure is subjected to a pre-annealing step to eliminate impurities from the electrode and thus overcome leakage problems which degrade the effectiveness of the capacitor. Since capacitor formation occurs in various heat environments, crystallization of the capacitor materials may occur. Capacitor materials have an inherent temperature of crystallization that is well known for a particular environment (e.g. heat under selected atmospheres). This is referred to as "conventional crystallization annealing" on page 7, line 17 of the application. The pre-annealing step, however, has the effect of lowering the crystallization temperature of the dielectric formed over the electrode, especially at the electrode-dielectric interface. The result is a crystallized dielectric layer which, in combination with an upper electrode and the pre-annealed lower electrode, form a capacitor structure that has many advantages over the prior art, including lower leakage current, higher capacitance per unit area, and no substantial change in materiality [see, e.g., FIG. 8A-8B].

substantial change in materiality [see, e.g., FIG. 8A-8B].

VI. ISSUES ON APPEAL
37 CFR §1.192(c) (6)

The issues on Appeal are as follows:

A. Whether "inherent temperature of crystallization is new matter or, in the alternative, whether the statement "conventional crystallization annealing temperature" is sufficiently clear to overcome §112, first paragraph issues of clarity; and

B. Whether all pending claims are non-obvious over the prior art, especially in view of the fact that the prior art (Agarwal) imposes a materiality change on the semiconductor structure, does not disclose a pre-anneal process for removing contaminations such as carbon from the lower electrode, and does not result in nearly the capacitance advantage as when the capacitor is formed using the present inventive methods.

VII. GROUPING OF CLAIMS
37 CFR §1.192(c) (7)

Claims 1, 13, and 20 are independent claims which are each independently patentable as incorporating different limitations. Claims 6, 17 stand or fall together. Claims 2 and 4 stand or fall with claim 1. Claims 7-12 stand of fall together. Claims 14-15 stand or fall with claim 13. Claims 24, 25 and 30-32 stand of fall together.

VIII. ARGUMENT
37 CFR §1.192(c) (8)

A. "Inherent Temperature of Crystallization Annealing" is Properly Understood to Mean "Conventional Crystallization Annealing Temperature"

Claims 7, 18, 24 and 25 are rejected under 25 USC §112, first paragraph, on the grounds that the specification does not provide support for the limitation.

On the contrary, the term "inherent temperature of crystallization annealing" should be well known to those skilled in the semiconductor and material science arts as the temperature at which a particular material by itself would undergo crystallization annealing. Use of the term "inherent" should not constitute new matter since such a term is well known in the art. An explanation of the difference between the crystallization temperature used in the inventive method and the *inherent* crystallization temperature of the material was described in previous responses. That is, it has been shown experimentally that the crystallization temperature for the dielectric is actually lower than the inherent crystallization temperature of the material due to formation of a dielectric (e.g. tantalum oxide) along a grain boundary of the pre-annealed lower electrode where the dielectric becomes partially crystallized. This partial crystallization decreases the crystallization temperature so that the actual crystallization temperature is lower than the inherent crystallization temperature.

In the March 3, 2003 Response, applicant stated:

> A further limitation, that of performing a "crystallization annealing" can be found in amended claims 7, 18, and to a more specific extent independent claim 20. Referring to the crystallization annealing of the capacitor dielectric layer, by the pre annealing, the crystallization temperature of the capacitor dielectric layer is lowered (see, e.g., page 7, line 16). That is, since the capacitor dielectric layer is grown along a grain boundary of the pre-annealed lower electrode, the capacitor dielectric layer becomes partially crystallized. This partial crystallization decreases the crystallization temperature. When the temperature of the crystallization of the capacitor dielectric layer is lowered, the leakage current substantially decreases, which is well known in the art. Such a matter is one of the features of the present invention. Therefore, the claims have been amended to reflect that the crystallization of the capacitor dielectric layer starts at a ***lower*** temperature than the *inherent crystallization* temperature of the capacitor dielectric layer (also claim 24).
>
> In claims 20 in particular, the capacitor dielectric layer claimed is a tantalum oxide layer. The inherent crystallization temperature of a tantalum oxide layer is over 700 C; however, the crystallization temperature of the tantalum oxide layer in the present invention is about 650 C. In contrast, the capacitor dielectric layer in the Aoki reference is PZT and the inherent crystallization temperature of PZT is about 650 C. Also, the Agarwal and Aoki references fail to disclose the crystallization of the capacitor dielectric layer at a lower temperature than the

> capacitor dielectric layer at a lower temperature than the inherent crystallization temperature of the capacitor dielectric layer. Therefore, the crystallization temperature of the present invention differs from that of the Aoki reference.

And in the subsequently filed Response:

> The term "inherent temperature of crystallization annealing" should be well known to those skilled in the semiconductor and material science arts as the temperature at which a particular material by itself would undergo crystallization annealing. Use of the term "inherent" should not constitute new matter since such a term is well known in the art. An explanation of the difference between the crystallization temperature used in the inventive method and the *inherent* crystallization temperature of the material was described in the previous response but is supplemented herein. That is, it has been shown experimentally that the crystallization temperature for the dielectric is actually lower than the inherent crystallization temperature of the material due to formation of a dielectric (e.g. tantalum oxide) along a grain boundary of the pre-annealed lower electrode where the dielectric becomes partially crystallized. This partial crystallization decreases the crystallization temperature so that the actual crystallization temperature is lower than the inherent crystallization temperature.

The specification as filed makes reference to the "conventional crystallization annealing temperature" on page 7, line 17. The "inherent" terminology is intended to be, and would be understood by those knowledgeable in the art to be, identical in scope and definition to the "conventional" language cited in the specification. The "inherency" language applies to crystallization temperatures of layers by themselves. As stated in the prior response, for instance, the inherent crystallization temperature of a tantalum oxide layer is over 700°C. And for a PZT layer, the inherent crystallization temperature is 650°C.

B. The Agarwal Prior Art and AAPA Cannot Be Properly Combined and Does Not Teach All Limitations of the Present Claims.

All claims have been rejected under 35 USC §103(a) as being unpatentable over Agarwal et al. (U.S. Pub. No. 2002/0037630) of record in view of Applicant's admitted prior art (AAPA). Not all limitations of the claims are taught or suggested by the prior art, however, and therefore rejection on these grounds is improper.

1. Applicable Law Concerning §103(a) Rejections

The Federal Circuit has been consistent in reversing the PTO when a rejection is made on the basis of hindsight, that is when an Examiner rejects the application under 35 U.S.C. §103(a) grounds as obvious under a combination of two or more patents without any specific suggestion within the patents to combine the features. In re Rouffett, 47 USPQ2d 1453 (Fed. Cir. 1998), the Federal Circuit refused

Federal Circuit refused to uphold an obviousness rejection, even where skill in the art is high, absent the specific identification of principal, known to one of ordinary skill in the art that suggests the claimed combination.

The Federal Circuit reemphasized the care to be taken when combining prior art references in obviousness findings in Ecolochem v. Southern Cal. Edison, 56 USPQ2d 1065 (Fed. Cir. 2000), stating that such absence of evidence to combine prior art references "is defective as hindsight analysis." The Federal Circuit held similarly in In re Kotzab, 55 USPQ2d 1313 (Fed. Cir. 2000), reversing the PTO and stating that, "[i]dentification of prior art statements that, in abstract, appear to suggest claimed limitation does not establish prima facie case of obviousness without finding as to specific understanding or principal within knowledge of skilled artisan that would have motivated one with no knowledge of the invention to make the combination in the manner claimed."

Finally, the Federal Circuit has reaffirmed their view that the PTO used improper hindsight analysis to reject patent claims under §103(a) in the recent case of In re Lee, 61 USPQ2d 1430 (Fed. Cir. 2002), stating that a specific suggestion in the prior art cited is required and not a simple citation to "common knowledge and common sense."

2. Agarwal Does Not Implicitly Refer to a Crystallized Dielectric Layer

Applicant can find no such specific recitation or suggestion within the reference regarding the use of a crystallized dielectric. Instead, paragraph 0048 of Agarwal '630 states only that the dielectric should have a high dielectric constant around 9, and that it be conformally formed as a "thin layer" over the enhanced surface area electrode (26) so that it preferably provides an enhanced surface area on a surface facing away from the bottom electrode. Paragraph 0055 states, in fact, that the anneal process is typically performed before the dielectric layer and second electrode are formed. And paragraph 0056 simply lists the suitable dielectric materials available.

The Examiner reads a limitation into the Agarwal reference that does not exist. Where the Agarwal reference refers to an increase in capacitance of 20% after the anneal process, this alone is not evidence that full crystallization of the dielectric occurs. Instead, experimentation has shown that the capacitance of the crystallized dielectric ***increases by about two to several tens of times***, general. That is, it is well known to those skilled in the art that the dielectric constant of the Ta_2O_5 layer increases by two times when Ta_2O_5 is crystallized and the dielectric constant of the ferroelectrics layer such as BST

constant of the ferroelectrics layer such as BST and STO increases by several tens of times. This is one or two orders of magnitude greater than the increase noted in Agarwal. As the dielectric constant increases, the capacitance increases in proportion to the dielectric constant. Thus in the Agarwal disclosure, the increase of the capacitance by about 20% indicates that the dielectric layer is not crystallized in a way that the present invention teaches, where (because of the pre-annealing) the crystallization occurs at temperatures lower than the conventional temperature of crystallization for the materials used.

3. *Agarwal Does Not Disclose a Pre-anneal Process for Removing Contaminations Such as Carbon*

The Examiner has focused on the claim 1 and 13 limitation "having carbon." But using such carbon source creates inherent disadvantages as expressed in the background of the invention section. That is,

> "according to the analysis of present inventors, the large leakage current problem in the capacitor having the lower electrode made by the CVD method is due to impurities, e.g., carbons. The impurities are produced in the lower electrode when the metal organic source gas is not completely decomposed during the CVD process for forming the lower electrode. The impurities are thought to suppress the crystallization of the capacitor dielectric layer. Moreover, the impurities may induce defects in the capacitor dielectric layer, even though the impurities are too small amount to be detected by SIMS (Secondary Ion Mass Spectrometry) analysis. The defects act as sources of the leakage current." (Present Application, page 1, line 32 to page 2, line 6).

It would not be obvious to use the CVD process using a source having carbon with the Agarwal process because of the inherent disadvantages. The pre-annealing process in the present invention is for the express purpose of alleviating this problem.

Agarwal, however, does not disclose a pre-annealing process for removing carbon and would not result in the removal of such. (see independent claims 1, 13 and 20) Instead, any pre-anneal process performed according to the teachings of Agarwal are for the purpose of and result in a conversion of the electrode composed of RuO into an electrode composed of Ru having surface morphology. Thus, the diffusion of oxygen (O) cannot be considered a release of contaminants.

4. *The Process of Agarwal Does in Fact Change the Material of the Lower Electrode*

Contrary to the limitations express in claims 6 and 17, the Agarwal reference changes the materiality of the lower electrode from RuO to Ru with surface morphology. This change is understood by those knowledgeable in the art to constitute a change in materiality. The Agarwal process would not result in the morphology shown in FIGs. 8A and 8B and thus does not suggest the same process.

IX. APPENDIX
37 CFR §1.192(c) (9)

The text of claims 1, 2, 4, 6-15, 17-20, 24, 25 and 30-32on appeal is:

1. (Previously amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate using a source having carbon;

subjecting the lower electrode to a pre-annealing for removing carbon remaining in the lower electrode, wherein the pre-annealing is a thermal annealing under a selected atmosphere;

forming a capacitor dielectric layer on the pre-annealed lower electrode, wherein the capacitor dielectric layer is formed of a crystalline material; and

forming an upper electrode on the capacitor dielectric layer,

wherein the lower electrode is formed of metal.

2. (Previously amended) The method of claim 1, wherein the lower electrode is formed of a material selected from the group consisting of ruthenium and platinum.

3. (Canceled)

4. (Previously amended) The method of claim 1, wherein a metal organic material is used as a source of the CVD method

5. (Canceled)

6. (Original) The method of claim 4, wherein the pre-annealing does not substantially change the materiality of the lower electrode.

7. (Currently amended) The method of claim 1, wherein the step of forming a capacitor dielectric layer comprises:

depositing a capacitor dielectric layer on the pre-annealed lower electrode wherein the deposited capacitor dielectric layer has an actual crystallization annealing temperature that is lower than an inherent crystallization temperature of the dielectric layer; and

after depositing the capacitor dielectric on the pre-annealed lower electrode, subjecting the capacitor dielectric layer to a temperature that is lower than the inherent temperature of the dielectric layer until a crystallization annealing of the dielectric layer occurs.

8. (Previously amended) The method of claim 6, wherein the pre-annealing is performed at a range of between 350 ~ 750°C.

9. (Original) The method of claim 4, wherein the selected atmosphere comprises a hydrogen gas.

10. (Original) The method of claim 4, wherein the selected atmosphere comprises a nitrogen gas.

11. (Original) The method of claim 4, wherein the selected atmosphere is a mixed atmosphere.

12. (Original) The method of claim 11, wherein the mixed atmosphere comprise a hydrogen and a nitrogen gas.

13. (Previously amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate by CVD method using a source having carbon;

subjecting the lower electrode to a pre-annealing for removing carbon remaining in the lower electrode, wherein the pre-annealing is a treatment exposing the lower electrode under a plasma atmosphere;

forming a capacitor dielectric layer on the pre-annealed lower electrode; and

forming an upper electrode on the capacitor dielectric layer,

wherein the lower electrode is formed of metal.

14. (Previously amended) The method of claim 13, wherein the lower electrode is formed of a material selected from the group consisting of ruthenium and platinum.

15. (Original) The method of claim 14, wherein a metal organic material is used as a source of the CVD method.

16. (Canceled)

17. (Original) The method of claim 15, wherein the pre-annealing does not substantially change the materiality of the lower electrode.

18. (Currently amended) The method of claim 13, wherein the step of forming a capacitor dielectric layer comprises:

depositing a capacitor dielectric layer on the pre-annealed lower electrode wherein the deposited capacitor dielectric layer has an actual crystallization annealing temperature that is lower than an inherent crystallization temperature of the dielectric layer; and

after depositing the capacitor dielectric on the pre-annealed lower electrode, subjecting the capacitor dielectric layer to a temperature that is lower than the inherent temperature of the dielectric layer until a crystallization annealing of the dielectric layer occurs.

19. (Original) The method of claim 15, wherein the plasma atmosphere comprises a hydrogen gas.

20. (Previously amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a lower electrode on a substrate by a CVD method using a source having carbon;

subjecting the lower electrode to a pre-annealing for removing carbon remaining in the lower electrode, wherein the pre-annealing is a treatment exposing the lower electrode under plasma atmosphere;

depositing a tantalum oxide layer on the pre-annealed lower electrode;

crystallizing the tantalum oxide layer at a crystallizing temperature; and

forming an upper electrode on the capacitor dielectric layer,

wherein the lower electrode is formed of metal, the pre-annealing is performed at a range of between 350 ~ 750°C, and the materiality and surface morphology of the lower electrode does not substantially change by the pre-annealing.

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Currently amended) The method of claim 20, wherein a temperature of the crystallization annealing is lower than the inherent temperature of crystallization of said capacitor dielectric layer.

25. (Currently amended) The method of claim 24, wherein the inherent crystallizing temperature of the tantalum oxide layer is 700°C and the crystallizing temperature of the tantalum oxide layer is about 650°C.

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Canceled)

30. (Previously amended) The method of claim 8, wherein the pre-annealing is performed at about 450°C.

31. (Previously amended) The method of claim 17, wherein the pre-annealing is performed at a range of between 350 ~ 750°C.

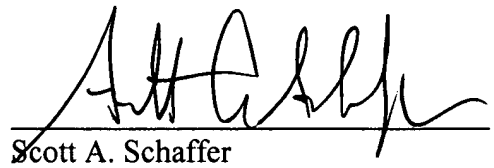
32. (Previously amended) The method of claim 31, wherein the pre-annealing is performed at about 450°C.

CONCLUSION

The Appellant requests favorable consideration by the Board. If any questions remain, please, the Board is encouraged to contact the undersigned at the number indicated below.

Respectfully submitted,

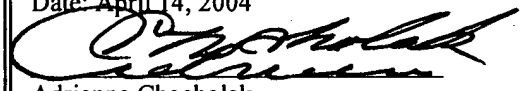
MARGER JOHNSON & McCOLLOM, P.C.



Scott A. Schaffer
Reg. No. 38,610

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
503-222-3613

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Appeal Brief – Patents; Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450
Date: April 14, 2004



Adrienne Chocholak